What is claimed is

1. A main word line driver circuit of a semiconductor memory device, the circuit generating main word line signals enabling a plurality of main word lines, respectively, comprising:

a voltage supply unit which supplies a first voltage to a node and then supplies a second voltage higher than the first voltage; and

a plurality of output units which receive the first voltage and second voltage supplied to the node and generate the respective main word line signals.

2. The circuit of claim 1, wherein the first voltage is a negative voltage and the second voltage is the ground voltage.

3. The circuit of claim 2, wherein the voltage supply unit comprises:

a negative voltage supply unit which supplies the negative voltage to the node; and

a ground voltage supply unit which supplies the ground voltage to the node.

4. The circuit of claim 3, wherein the negative voltage supply unit supplies the negative voltage to the node in response to activation of decoded row address signals.

5. The circuit of claim 4, wherein one of the decoded row address signals is activated as the supply voltage for a predetermined time interval.

6. The circuit of claim 5, wherein the negative voltage supply unit comprises three NMOS transistors which are serially connected and turned on/off in response to the decoded row address signals, and the negative voltage is connected to an end of the NMOS transistors.